2 T885 Circuit Operation

This section provides a basic description of the circuit operation of the T885 receiver.

Note: Unless otherwise specified, the term "PGM800Win" used in this and following sections refers to version 3.00 and later of the software.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB.

The following topics are covered in this section.

Section	Title	Page
2.1	**Introduction**	**2.3**
2.2	**Receiver Front End**	**2.4**
2.3	**Mixer**	**2.5**
2.4	**IF Circuitry**	**2.5**
2.5	**Noise Mute (Squelch)**	**2.6**
2.6	**Carrier Mute**	**2.6**
2.7	**Audio Processor**	**2.7**
2.8	**Power Supply And Regulators**	**2.8**
2.9	**Microcontroller**	**2.9**
2.10	**Synthesised Local Oscillator**	**2.10**
2.11	**VCO**	**2.11**
2.12	**Received Signal Strength Indicator (RSSI)**	**2.12**

Figure	Title	Page
2.1	T885 High Level Block Diagram	2.3
2.2	T885 Front End, IF and Mute Block Diagram	2.4
2.3	T885 Audio Processor Block Diagram	2.7
2.4	T885 Power Supply And Regulators Block Diagram	2.8
2.5	T885 Microcontroller Block Diagram	2.9
2.6	T885 Synthesiser Block Diagram	2.10
2.7	T885 RSSI Block Diagram	2.12

2.1 Introduction

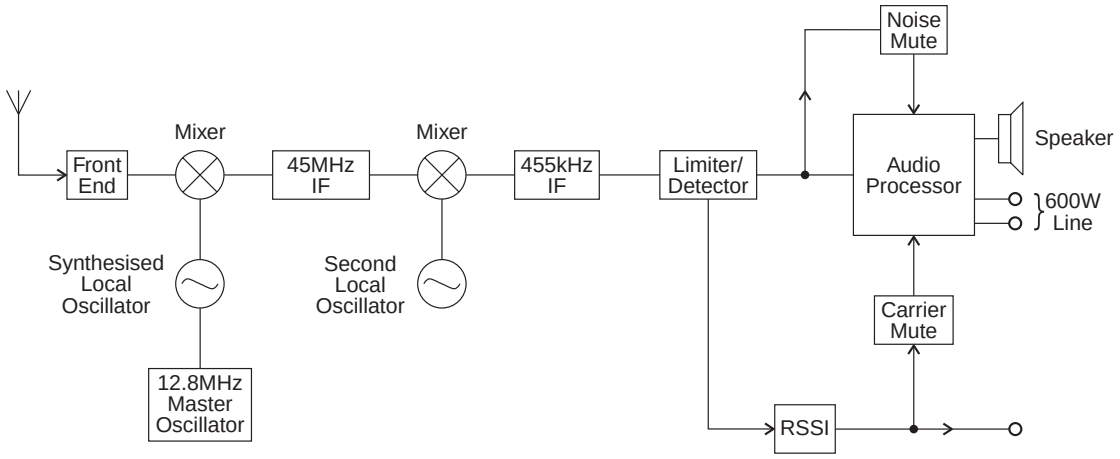

Figure 2.1 T885 High Level Block Diagram

The T885 receiver consists of a number of distinct stages:

- front end
- mixer
- synthesised local oscillator
- IF
- audio processor
- mute (squelch)
- regulator circuits
- received signal strength indicator (RSSI).

These stages are clearly identifiable in Figure 2.1. Refer to the circuit diagrams in Section 6 for further detail.

2.2 Receiver Front End

(Refer to the front end, IF section and audio processor circuit diagrams (sheets 4, 3 and 2 respectively) in Section 6.2.)

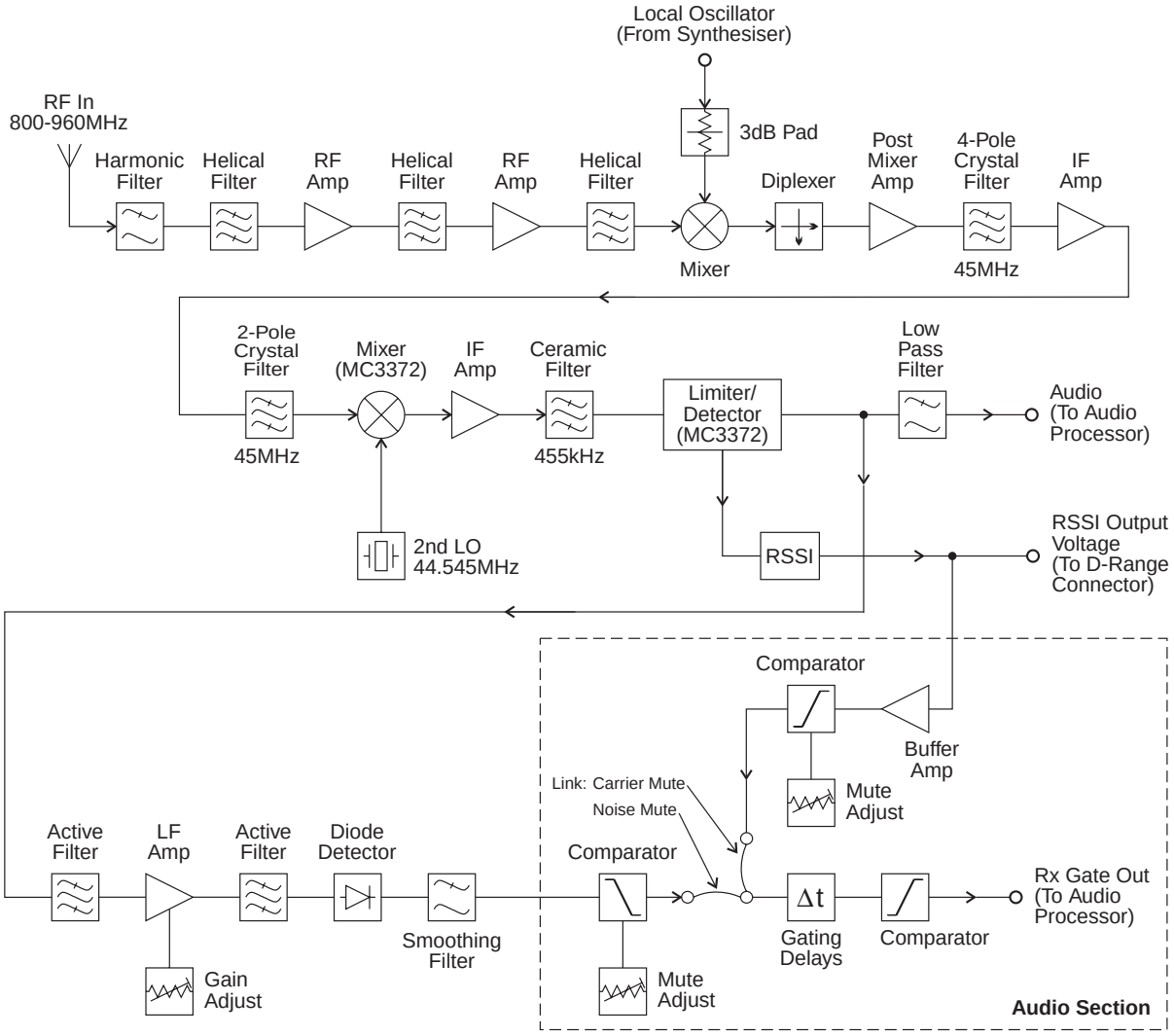

Figure 2.2 T885 Front End, IF and Mute Block Diagram

The incoming signal from the N-type antenna socket is fed through a 7-pole, low pass filter with a cut frequency of approximately 1.2GHz. This low loss filter (typically less than 0.5dB over 800-960MHz) provides excellent immunity to interference from high frequency signals.

The signal is filtered again, using a high performance helical resonator doublet (#H900) which provides exceptional image rejection, before being amplified by approximately 7dB (Q401). The signal is then passed through a further helical filter doublet (#H400), after which it is amplified again by 8dB (Q403). It is finally filtered by #H401 before being presented to the mixer.

Each sub-block within the front end has been designed with 50 ohm terminations for ease of testing and fault finding. The overall gain from the antenna socket to the mixer input is approximately 8dB.

2.3 Mixer

(Refer to the front end circuit diagram (sheet 4) in Section 6.2 and Figure 2.2.)

IC410 is a high level mixer requiring a local oscillator (LO) drive level of +17dBm (nominal). The voltage controlled oscillator (VCO) generates a level of +20dBm (typical) and this is fed to the mixer via a 3dB attenuator pad. A diplexer terminates the IF port of the mixer in a good 50 ohms, thus preventing unnecessary intermodulation distortion.

2.4 IF Circuitry

(Refer to the IF section circuit diagram (sheet 3) in Section 6.2 and Figure 2.2.)

Losses in the mixer are made up for in a tuned, common gate, post mixer amplifier (Q300). Several stages of amplification and filtering are employed in the IF circuitry. The first crystal filter is a 4-pole device (&XF300) which is matched into 50 ohms on its input and directly to the impedance of the next stage on its output. This stage is followed by a cascode amplifier (Q302) whose output is matched into a 2-pole crystal filter (&XF302). The signal is then mixed down to 455kHz with the second crystal local oscillator (44.545MHz).

The 455kHz signal is filtered using a 6-pole ceramic filter (IC345) before being limited and detected.

The second IF mixer, limiter and detector is in a 16-pin IC (IC300). This IC also provides an RSSI signal on pin 13. Quadrature detection is employed, using L345, and the recovered audio on pin 9 of IC300 is typically 1V p-p for 60% system deviation.

2.5 Noise Mute (Squelch)

(Refer to the audio processor and IF section circuit diagrams (sheets 2 and 3 respectively) in Section 6.2 and Figure 2.2.)

The noise mute operates on the detected noise outside the audio bandwidth. Two operational amplifiers in IC330 are used as an active band-pass filter centred on 70kHz to filter out audio components and provide gain. Between the active filter stages is a variable gain stage which utilises one of the remaining operational amplifiers in IC330. The noise is then rectified (D330) and filtered to produce a DC voltage proportional to the noise amplitude. The lowest average DC voltage corresponds to a high RF signal strength and the highest DC voltage corresponds to no signal at the RF input.

The rectified noise voltage is compared with a threshold voltage set up on RV230, the front panel "Gating Sensitivity" potentiometer. Hysteresis is provided by the feedback resistor (R267) to prevent the received message from being chopped when the average noise voltage is close to the threshold. R281 and R280 determine the mute opening and closing times and, in combination with solder links SL210 and SL220, provide three time delay options (SL210 is linked as standard - refer to Section 3.8). The mute control signal at pin 7 of IC270 is used to disable the speaker and line audio outputs. The speaker output can be separately enabled for test purposes by operating the front panel mute disable switch, SW201.

2.6 Carrier Mute

(Refer to the audio processor and IF section circuit diagrams (sheets 2 and 3 respectively) in Section 6.2 and Figure 2.2.)

A high level carrier mute facility is also available. The RSSI (refer to Section 2.12) provides a DC voltage proportional to the signal strength. This voltage is compared with a preset level, set up on RV235, and may be linked into the mute timing circuit using PL250. PL250 selects either the noise mute or the carrier mute. From this point both the noise and carrier mute circuits operate in the same manner, using common circuitry.

2.7 Audio Processor

(Refer to the audio processor circuit diagram (sheet 2) in Section 6.2.)

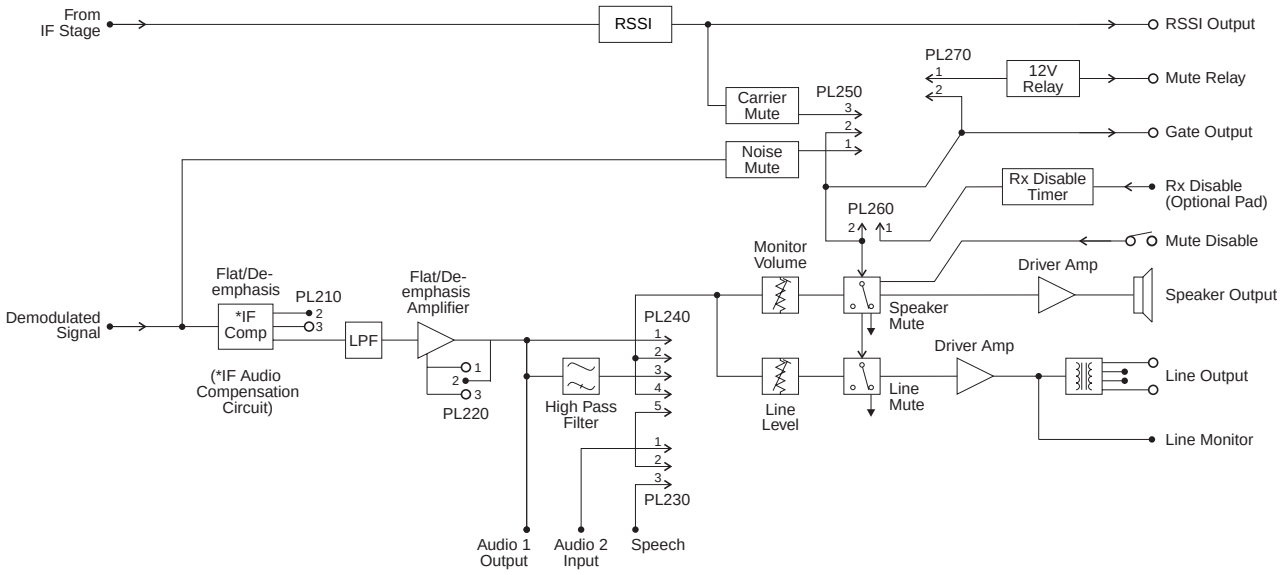

Figure 2.3 T885 Audio Processor Block Diagram

The recovered audio on pin 9 of IC310 is passed through a compensation network and processed in a third order elliptic active filter to give the required response. Linking (PL220 & PL210) is available to give either a flat or de-emphasised audio response, with de-emphasis giving a -6dB/octave roll off. The output of IC210 is split to provide separate paths for the speaker and line outputs. The "Audio 1", Audio 2" and "Speech" lines allow access to the receiver's audio path for external signalling purposes (refer to Section 3.5).

The signals are passed to audio drive amplifiers IC240 and IC260. Under muted conditions the inputs of these amplifiers are shunted to ground via transistors Q230 and Q290 respectively. The audio output of IC240 has a DC component which is removed by C249, and this then drives a speaker directly. The output of IC260 is fed into a line transformer to provide a balanced 2-wire or 4-wire, 600 ohm output.

The speaker volume is set using the front panel "Monitor Volume" knob (RV205) and the line level is set using the recessed "Line Level" potentiometer (RV210).

The red front panel "Gate" LED (D250) indicates the status of the mute circuit. When a signal above the mute threshold is received, the LED is illuminated. The "Monitor Mute" switch (SW201) on the front panel opens the mute, allowing continuous monitoring of the audio signal (on = audio muted; off = audio unmuted).

The mute control line is available on pad 234 ("RX GATE OUT") for control of external circuitry. A high (9V) on pad 234 indicates that the audio is disabled and a low (0V) indicates that a signal above the mute threshold level is being received.

The audio can also be disabled using the "RX-DISABLE" inputs, pads 225 or 228, having connected the "RX-DISABLE" link between pins 1 & 2 of PL260. An adjustable time delay (RV220) is provided on these lines. In order to disable the audio, either pad must be pulled to 0V.

An undedicated relay is provided (RL210) for transmitter keying or other functions and this can be operated from the mute line by linking PL270.

2.8 Power Supply And Regulators

(Refer to the regulators circuit diagram (sheet 6) in Section 6.2.)

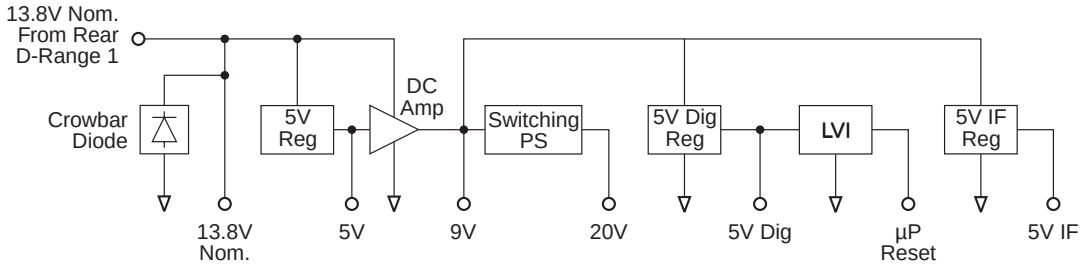

Figure 2.4 T885 Power Supply And Regulators Block Diagram

The T885 is designed to operate off a 10.8-16V DC supply (13.8V nominal). A 5.3V regulator (IC630) runs directly from the 13.8V rail, driving much of the synthesiser circuitry. It is also used as the reference for a DC amplifier (IC640, Q630 & Q620) which provides a medium current capability 9V supply.

A switching power supply, based on Q670 and Q660, runs off the 9V supply and provides a low current capability +20V supply. This is used to drive the synthesiser loop filter (IC740), giving a VCO control voltage of up to 20V.

The 13.8V supply drives both output audio amplifiers without additional regulation. A separate 5V regulator (IC610) drives the microprocessor and associated digital circuitry. The output of this regulator is monitored by the Low Voltage Interrupt (LVI) circuit (IC650). An additional 5V regulator (located in the IF cavity) supplies the first IF amplifier (Q301, Q302) and the demodulator IC (IC300).

A crowbar diode is fitted for protection against connection to a power supply of incorrect polarity. It also provides transient overvoltage protection.

Note: A fuse must be fitted in the power supply line for the diode to provide effective protection.

2.9 Microcontroller

(Refer to the microcontroller circuit diagram (sheet 8) in Section 6.2.)

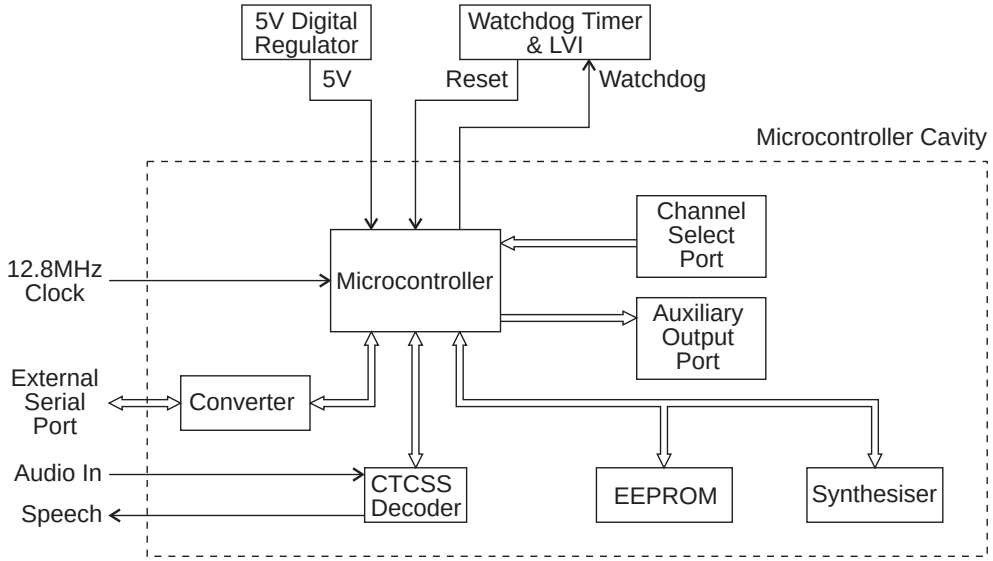

Figure 2.5 T885 Microcontroller Block Diagram

Overall system control of the T885 is accomplished by the use of a member of the 80C51 family of microcontrollers (IC810) which runs from internal ROM and RAM. Four ports are available for input/output functions.

Non-volatile data storage is achieved by serial communication with a 16kBit EEPROM (IC820). This serial bus is also used by the microcontroller to program the synthesiser (IC740).

The main tasks of the microcontroller are as follows:

- program the synthesiser;
- interface with the PGM800Win programming software at 9600 baud via the serial communication lines on D-range 1 (PL100) & D-range 2;
- monitor channel change inputs from D-range 2;
- generate timing waveforms for CTCSS detection;
- coordinate and implement timing control of the receiver;
- control the front panel "Supply" LED.

2.10 Synthesised Local Oscillator

(Refer to the synthesiser circuit diagram (sheet 7) and the VCO circuit diagram (sheet 5) in Section 6.2.)

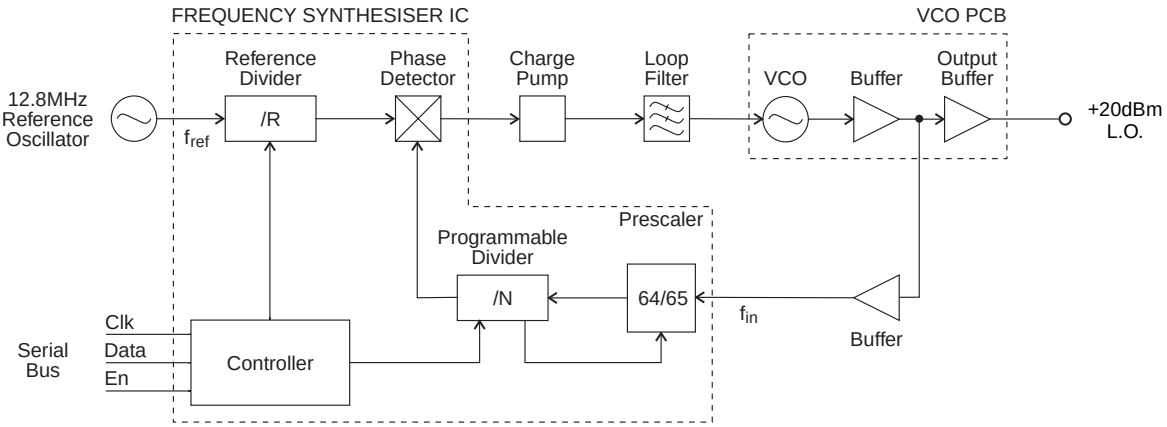

Figure 2.6 T885 Synthesiser Block Diagram

The synthesiser (IC740) employs a phase-locked loop (PLL) to lock a voltage controlled oscillator (VCO) to a given reference frequency. The synthesiser receives the divider information from the control microprocessor via a 3-wire serial bus (clock, data, enable). When the data has been latched in, the synthesiser processes the incoming signals from the VCO buffer (f_{in}) and the reference oscillator (f_{ref}).

A reference oscillator at 12.8MHz (IC700) is buffered (IC710) and divided down to 6.25kHz or 5kHz within the synthesiser IC (IC740).

A buffered output of the VCO is divided with a prescaler and programmable divider which is incorporated into the synthesiser chip (IC740). This signal is compared with the reference signal at the phase detector (also part of the synthesiser chip). The phase detector outputs drive a balanced charge pump circuit (Q760, Q770, Q775, Q780, Q785) and active loop filter (IC750, Q790) which produces a DC voltage between 0V and 20V to tune the VCO. This VCO control line is further filtered to attenuate noise and other spurious signals. Note that the VCO frequency increases with increasing control voltage.

2.11 VCO

(Refer to the VCO circuit diagram (sheet 5) in Section 6.2.)

The VCO consists of several stages: oscillator, cascode buffer, broadband amplifier and output buffer. The oscillator transistor (Q504) operates in a common base Colpitts configuration and is capacitively coupled to a short-circuited coaxial resonator (&TL500). The resonator frequency is capacitively tuned by varicaps (D501, D502, D509, D505) and coarse manual tuning is provided by the sapphire trimcap (CV500).

The cascode buffer (Q540, Q541) provides the signal to the divider buffer in the synthesiser circuit as well as 0dBm to the broadband amplifier (Q543). The broadband amplifier provides +10dB of gain, as does the output buffer stage (T540), which brings the VCO output up to +20dBm.

The VCO operates at the actual frequency required by the first mixer, i.e. there are no multiplier stages.

The VCO frequency spans from either 755-825MHz, 815-865MHz or 845-915MHz according to product type (refer to Section 1.4). The VCO is tuned to 45MHz below the desired receive frequency (low side injection) to produce a 45MHz IF signal at the output of the mixer.

2.12 Received Signal Strength Indicator (RSSI)

(Refer to the IF section circuit diagram (sheet 3) in Section 6.2.)

The RSSI provides a DC voltage proportional to the signal level at the receiver input and is an on-chip function of the demodulator IC (IC300). Circuitry external to IC300 conditions the RSSI signal and the voltage is available at D-range 1 (PL100 pin 5).

The RSSI also provides the capability for high level signal strength muting, which may be selected on PL250 (refer to Section 3.5). The mute threshold may be set between -115dBm and -70dBm by RV235.

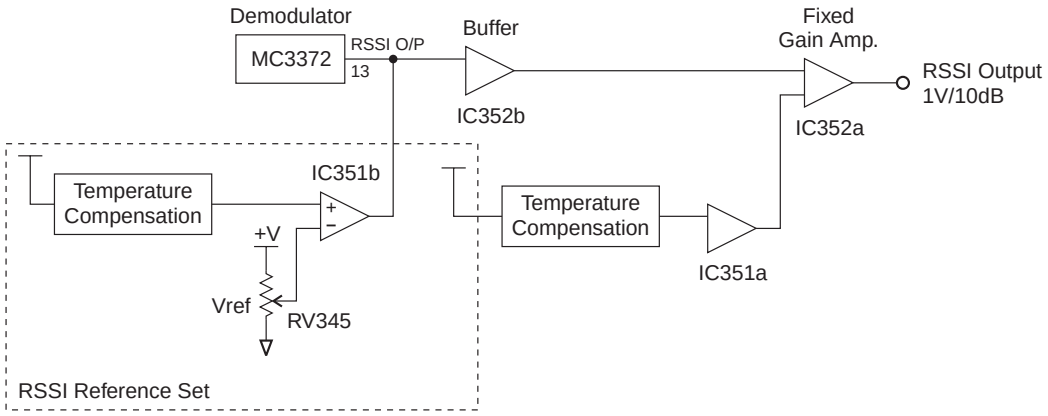

Figure 2.7 T885 RSSI Block Diagram

The voltage offset of the RSSI signal (IC300 pin 13) is adjusted by RV345. This adjustment is temperature compensated by an operational amplifier (IC351b). The signal passes through a buffer amplifier (IC352b) before being amplified (IC352a) to give the correct volts per dB. The amplifier is temperature compensated by IC351a and its associated circuitry.

